Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (canceled)

Claim 2 (canceled)

Claim 3 (canceled)

Claim 4 (previously presented): The method of claim 21 wherein power is cut and then restored to at least a first traction motor, while maintaining constant power to the remaining motors, to correct loss of traction on an individual motor.

Claim 5 (previously presented): The method of claim 21 wherein over-current protection for each individually controlled direct current motor is provided.

Claim 6 (previously presented): The method of claim 21 wherein power is also provided to all motors constantly at reduced voltage difference during selected intervals.

Claim 7 (canceled)

Claim 8 (previously presented): The apparatus of claim 20 wherein said sequencer

comprises a pulse width modulation device.

Claim 9 (previously presented): The apparatus of claim 8 wherein said sequencer further comprises a clock.

Claim 10 (previously presented): The apparatus of claim 20 wherein said sequencer comprises a plurality of drive switches.

Claim 11 (previously presented): The apparatus of claim 20 wherein said controller comprises a programmable logic controller.

Claim 12 (previously presented): The apparatus of claim 20 wherein said controller comprises a throttle.

Claim 13 (previously presented): The apparatus of claim 20 wherein said controller comprises a power source current sensing device and a power source voltage sensing device.

Claim 14 (previously presented): The apparatus of claim 20 wherein said controller comprises a traction motor current sensing device.

Claim 15 (previously presented): The apparatus of claim 20 wherein said controller comprises a ramping device.

Claim 16 (previously presented): The apparatus of claim 20 wherein said controller comprises a detection scaling device.

Claim 17 (previously presented): The apparatus of claim 20 wherein said controller comprises a derate evaluation logic device.

Claim 18 (previously presented): The apparatus of claim 10 wherein said drive switches are insulated gate bipolar transistors.

Claim 19 (previously presented): The apparatus of claim 10 further comprising latching circuit means adapted to interrupt the drive of said drive switch after said drive switch has failed to fully saturate to thereby prevent operating into a short circuit.

Claim 20 (previously presented): An apparatus for controlling power provided from a direct current power source to a plurality of direct current traction motors, comprising:

(a) a controller operable to determine the power requirement for each motor at each of a number of successive time intervals and determine the necessary amplitude and pulse width of a power pulse to achieve the desired power for each motor; and

(b) a sequencer operable to sequentially pulse power to each said motor for a duration necessary to achieve said power requirement at said time interval, wherein, when the revolutions per minute (RPM) of each of the traction motors is below an intermediate RPM threshold, the pulses provided to the direct current traction motors are temporally non-overlapping and, when the RPM of each of the traction motors is above the intermediate RPM threshold, the pulses provided to the direct current traction motors are temporally at least partially overlapping.

Claim 21 (previously presented): A method of controlling power provided from a direct current power source to a plurality of direct current traction motors, comprising:

(a) determining the power requirement for each motor at each of a number of successive time intervals;

(b) determining the necessary effective amplitude and pulse width of a power pulse to achieve the desired power for each motor; and

(c) sequentially pulsing power to each said motor for a duration necessary to achieve said power requirement at said time interval, wherein, when the revolutions per minute (RPM) of each of the traction motors is below an intermediate RPM threshold, the pulses provided to the direct current traction motors are temporally non-overlapping and, when the RPM of each of the traction motors is above the intermediate RPM threshold, the pulses provided to the direct current traction motors are temporally at least partially overlapping.

Claim 22 (previously presented): A method of controlling power provided from a direct current power storage source to a plurality of direct current traction motors, comprising:

(a) determining the power requirement for each motor at each of a number of successive time intervals;

(b) determining the necessary effective amplitude and pulse width of a power pulse to achieve the desired power for each motor; and

(c) sequentially pulsing power to each said motor for a duration necessary to achieve said power requirement at said time interval, wherein, for each motor, the frequency of pulses is maintained at least substantially constant and wherein the pulse width is varied depending upon the revolutions per minute of the respective traction motor.

Claim 23 (previously presented): The method of claim 22, wherein a temporal spacing between adjacent pulses to each motor is maximized.

Claim 24 (previously presented): The method of claim 22 wherein power is cut and then restored to at least a first traction motor, while maintaining constant power to the remaining motors, to correct loss of traction on an individual motor.

Claim 25 (previously presented): The method of claim 22 wherein over-current protection for each individually controlled direct current motor is provided.

Claim 26 (previously presented): The method of claim 22 wherein power is also provided to all motors constantly at reduced voltage difference during selected intervals.

Claim 27 (previously presented): An apparatus for controlling power provided from a direct current power storage source to a plurality of direct current traction motors, comprising:

(a) a controller operable to determine the power requirement for each motor at each of a number of successive time intervals and determine the necessary amplitude and pulse width of a power pulse to achieve the desired power for each motor; and

(b) a sequencer operable to sequentially pulse power to each said motor for a duration necessary to achieve said power requirement at said time interval, wherein, for each motor, the frequency of pulses is maintained at least substantially constant and wherein the pulse width is varied depending upon the revolutions per minute of the respective traction motor.

Claim 28 (previously presented): The apparatus of claim 27, wherein a temporal

spacing between adjacent pulses to each motor is maximized.

Claim 29 (previously presented): The apparatus of claim 27 wherein said sequencer comprises a pulse width modulation device.

Claim 30 (previously presented): The apparatus of claim 29 wherein said sequencer further comprises a clock.

Claim 31 (previously presented): The apparatus of claim 27 wherein said sequencer comprises a plurality of drive switches.

Claim 32 (previously presented): The apparatus of claim 27 wherein said controller comprises a programmable logic controller.

Claim 33 (previously presented): The apparatus of claim 27 wherein said controller comprises a throttle.

Claim 34 (previously presented): The apparatus of claim 27 wherein said controller comprises a power source current sensing device and a power source voltage sensing device.

Claim 35 (previously presented): The apparatus of claim 27 wherein controller comprises a traction motor current sensing device.

Claim 36 (previously presented): The apparatus of claim 27 wherein said controller comprises a ramping device.

Claim 37 (previously presented): The apparatus of claim 27 wherein said controller comprises a detection scaling device.

Claim 38 (previously presented): The apparatus of claim 27 wherein said controller comprises a derate evaluation logic device.

Claim 39 (previously presented): The apparatus of claim 31 wherein said drive switches are insulated gate bipolar transistors.

Claim 40 (previously presented): The apparatus of claim 31 further comprising latching circuit means adapted to interrupt the drive of said drive switch after said drive switch has failed to fully saturate to thereby prevent operating into a short circuit.

Claim 41 (currently amended): A method of controlling power provided from a direct current power source to a plurality of direct current traction motors, comprising:

(a) determining that at least a first traction motor is experiencing wheel slip while each of the remaining traction motors are not experiencing wheel slip; and

(b) in response to the determining step, terminating power to the at least a first traction motor while continuing to provide power pulses to the remaining traction motors; and

(c) sequentially pulsing power to each said traction motor for a duration sufficient to achieve a selected power requirement for each traction motor during a selected time interval, wherein, for each motor, the frequency of pulses is maintained at least substantially constant and wherein the pulse width is varied depending upon the revolutions per minute of the respective traction motor.

Claim 42 (previously presented): The method of claim 41, wherein a temporal spacing between adjacent pulses to each motor is maximized.

Claim 43 (previously presented): The method of claim 41 wherein power is cut and then restored to at least a first traction motor, while maintaining constant power to the remaining motors, to correct loss of traction on an individual motor.

Claim 44 (previously presented): The method of claim 41 wherein over-current protection for each individually controlled direct current motor is provided.

Claim 45 (previously presented): The method of claim 41 wherein power is also provided to all motors constantly at reduced voltage difference during selected intervals.

Claim 46 (currently amended): An apparatus for controlling power provided from a direct current power source to a plurality of direct current traction motors, comprising:

a controller operable to (a) determine that at least a first traction motor is experiencing wheel slip while each of the remaining traction motors are not experiencing wheel slip and (b), in response to the wheel slip determination, terminate power to the at least a first traction motor while continuing to provide power pulses to the remaining traction motors;

and further comprising a sequencer operable to sequentially pulse power to each said motor for a duration necessary to achieve a selected power requirement at a selected time interval, wherein, for each motor, the frequency of pulses is maintained at least substantially constant and wherein the pulse width is varied depending upon the revolutions per minute of the respective traction motor.

Claim 47 (canceled)

Claim 48 (currently amended): The apparatus of claim ~~47~~ 46, wherein a temporal spacing between adjacent pulses to each motor is maximized

Claim 49 (currently amended): The apparatus of claim ~~47~~ 46 wherein said sequencer comprises a pulse width modulation device.

Claim 50 (currently amended): The apparatus of claim ~~47~~ 46 wherein said sequencer further comprises a clock.

Claim 51 (currently amended): The apparatus of claim ~~47~~ 46 wherein said sequencer comprises a plurality of drive switches.

Claim 52 (previously presented): The apparatus of claim 46 wherein said controller comprises a programmable logic controller.

Claim 53 (previously presented): The apparatus of claim 46 wherein said controller comprises a throttle.

Claim 54 (previously presented): The apparatus of claim 46 wherein said controller comprises a power source current sensing device and a power source voltage sensing device.

Claim 55 (previously presented): The apparatus of claim 46 wherein controller comprises a traction motor current sensing device.

Claim 56 (previously presented): The apparatus of claim 46 wherein said controller comprises a ramping device.

Claim 57 (previously presented): The apparatus of claim 46 wherein said controller comprises a detection scaling device.

Claim 58 (previously presented): The apparatus of claim 46 wherein said controller comprises a derate evaluation logic device.

Claim 59 (previously presented): The apparatus of claim 51 wherein said drive switches are insulated gate bipolar transistors.

Claim 60 (previously presented): The apparatus of claim 51 further comprising latching circuit means adapted to interrupt the drive of said drive switch after said drive switch has failed to fully saturate to thereby prevent operating into a short circuit.